I Claim:

1. A photosensitive array comprised of a plurality of pixels arranged in columns and rows, wherein the pixels are configured such that each said pixel has two transistors; including

a pixel output transistor having a sense electrode and an output elecrode;

a reset transistor having a gate couled to receive a reset signal and an output coupled to the sense electrode of the associated pixel output transistor; and

each said pixel also including a photosensitive element having an output electrode coupled to the sense electrode of the pixel output transistor.

2. A photosensitive array according to Claim 1 wherein the photosensitive element of each said pixel includes a photogate that captures and accumulates photon-generated charge; a sense gate positioned on said photogate; and a sense node that surrounds the photogate.

3. A photosensitive array comprised of a plurality of pixels arranged in columns and rows, wherein the pixels are configured into groups of at least a first pixel and a second pixel, each said group including

a shared pixel output transistor having a sense electrode and an output electrode;

a reset transistor having a gate coupled to receive a reset signal and an output coupled to the sense electrode of the associated shared pixel output transistor; and

each of said first and second pixels including a photosensitive element having an output electrode coupled to the sense electrode of the shared pixel output

transistor and a gate electrode coupled to receive respective first and second pixel gating signals.

4. A photosensitive array according to Claim 3 wherein said first and second pixels of each said group are both disposed in the same column.

5. A photosensitive array according to Claim 3 wherein the first and second pixels of each said group are disposed in successive columns in a single row.

6. A photosensitive array according to Claim 3 wherein the photosensitive element of each said pixel includes a photogate that captures and accumulates photon generated charge; a sense gate positioned on said photogate; and a sense node that surrounds the photogate.

7. A photosensitive array according to Claim 6 wherein the photosensitive elements of said first and second pixels are adjacent one another and the sense nodes thereof share a segment in common with one another.

8. A photosensitive array according to Claim 3 wherein each said photosensitive element includes a sense node FET having a gate electrode.

9. A photosensitive array according to Claim 3 wherein each said photosensitive element is formed of a charge snare device.

10. A photosensitive array according to Claim 3 wherein each said photosensitive element is formed of a photogate and a transfer gate, wherein one electrode of a transfer transistor thereof is connected to a photodiode and another electrode thereof is connected to said sense electrode, and a gate of said transfer transistor is connected to receive a control signal to operate timing of transfer and reset of said photodiode.

11. A photosensitive array according to Claim 3 wherein seach said photosensitive element is formed of a photodiode and a transfer gate.

12. A photosensitive array according to Claim 11 wherein one electrode transfer transistor of said transfer gate is connected to a photodiode and another electrode is connected to said sense electrode, and a gate of said transfer transistor is connected to receive a control signal to operate timing of transfer and reset of said photodiode.

13. A photosensitive array according to Claim 3 further comprising color filters on said first and second photosensitive elements.

14. A photosensitive array according to Claim 3 wherein said groups each include a third pixel and a fourth pixel, each of which includes a photosensitive element having an output electrode coupled to the sense electrode of said shared pixel output transistor, and a gate electrode to receive a respective gating signal.

15. A photosensitive array according to Claim 14 wherein said groups each include

a second reset transistor.

16. A photosensitive array according to Claim 3 wherein said groups each include a third and fourth pixel, each of which includes a photosensitive element having an output electrode, and a gate electrode to receive a respective gating signal; a second pixel output transistor having a sense electrode coupled to the output electrodes of the third and fourth pixel photosensitive elements; and a second reset transistor having a gate coupled to receive a second reset signal and an output coupled to the sense electrode of said second pixel output transistor.

17. A photosensitive array according to Claim 3 wherein said reset transistor is an FET having a drain thereof connected to the sense electrode of said pixel output transistor.

18. A photosensitive array according to Claim 17 wherein said pixel output transistor includes an FET having its gate electrode connected to the drain of the FET of said reset transistor.

19. A photosensitive array according to Claim 3 wherein said group includes at least a third pixel with the third pixel also sharing said pixel output transistor.

20. A photosensitive array according to Claim 3, wherein said group includes first, second, third, and fourth pixels, in a 2X2 arrangement, all sharing said pixel output transistor.